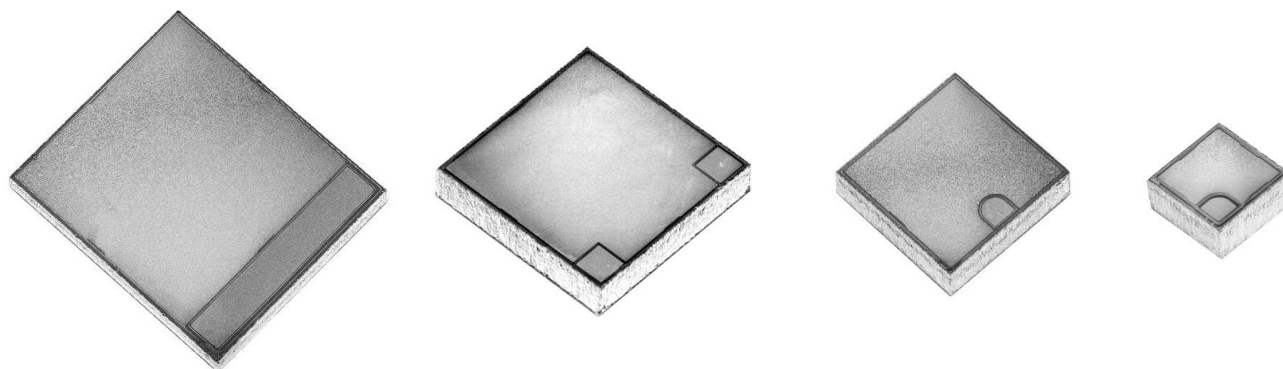


# Cree® EZ-p™ LED Chips

## Handling and Packaging Recommendations

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### INTRODUCTION

This application note provides the user with an understanding of Cree's EZ-p™ p-pad up (anode up) LED devices, as well as recommendations on handling and packaging. Further details regarding performance and dimensional specifications of EZ-p LED chips can be found at <http://www.cree.com/led-chips/products>.

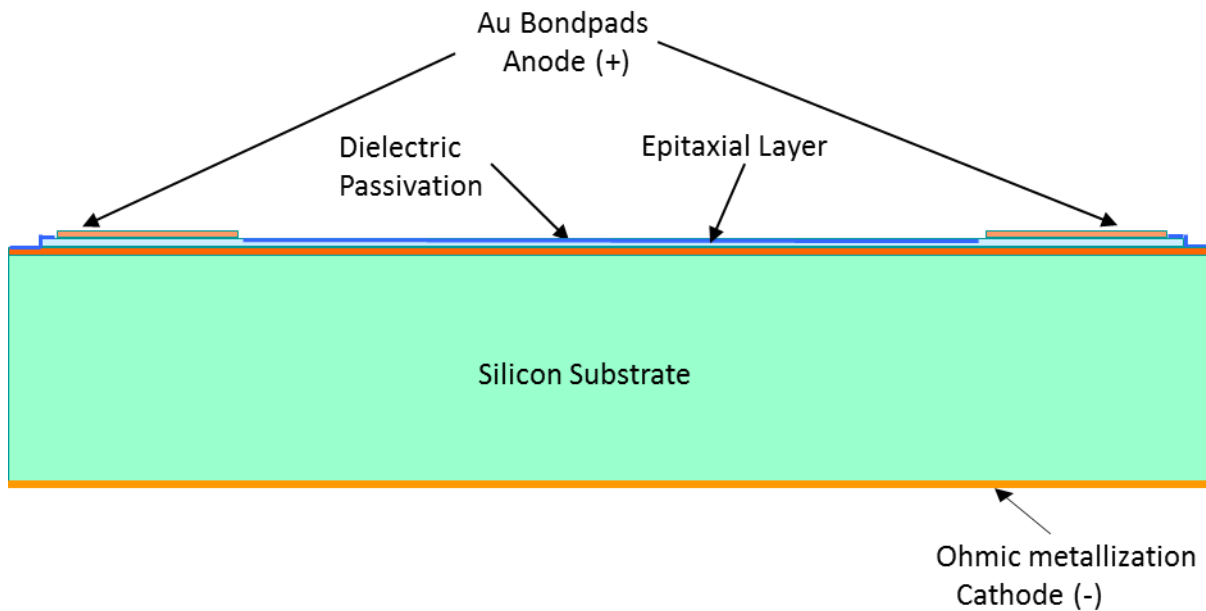
### TABLE OF CONTENTS

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EZ-p LED STRUCTURE .....	2
EZ-p LED CHIP HANDLING .....	3
Die Ejection.....	3
Collets.....	4
EZ-p LED CHIP DIE ATTACH .....	5
Eutectic/Solder Attach.....	5
Flux.....	5
Reflow.....	6
Adhesive Attach .....	7
EZ-p LED WIRE BONDING .....	8

**EZ-p LED STRUCTURE**

A cross-sectional schematic diagram of an EZ-p LED is shown below. The EZ-p LED has a vertical structure with topside Au bond pad anode (+) terminals and an Ohmic metal cathode (-) on the bottom of the silicon substrate. The epitaxial emitting layer is metallurgically bonded to the silicon substrate and the surface of the emitting area is passivated. For more detailed dimensional information and operational characteristics for the full line of EZ-p LEDs please consult the specification documents at the Cree website: <http://www.cree.com/led-chips/products>.



**EZ-p LED CHIP HANDLING**

In general, industry standard handling procedures can be used with the EZ-p LED. Both coaxial and radial lighting sources (ring or fiber lights) are recommended for pattern recognition systems in automated pick and place or bonding processes. Low angle side lighting may also be used to provide improved contrast.

The following guidelines include recommendations to maintain optimal performance:

- Minimize contact between metallic fixtures, equipment, tweezers, or other hard objects and the emitting surface or the edge of the emitting layer, as excessive contact force can damage the device, leading to electrical leakage and reduced optical output.
- If possible, avoid application of tapes or adhesives to the emitting surface. Tape residue can contaminate the textured surface, leading to reduced light extraction efficiency or poor lamp encapsulant adhesion.

*Die Ejection*

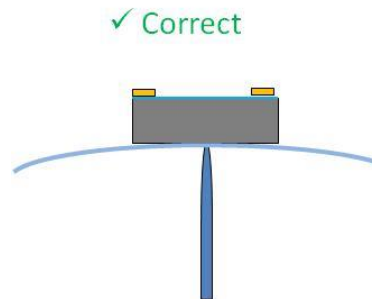
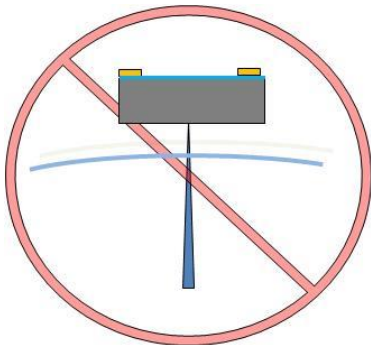
EZ-p LED chips are shipped from Cree with the epitaxial side up on the carrier tape. The application of excessive force during the die ejection process must be avoided. To minimize the risk of damage Cree recommends the following:

- Observe the following ejector pin minimum tip radius guidelines (Table 1)

EZ-p Chip	Minimum Tip Radius ( $\mu\text{m}$ )
Chip dimension < 400 $\mu\text{m}$	22
400 $\mu\text{m}$ $\leq$ Chip dimension $\leq$ 1000 $\mu\text{m}$	50
Chip dimension > 1000 $\mu\text{m}$	125

**Table 1: Recommended minimum ejector pin tip radius**

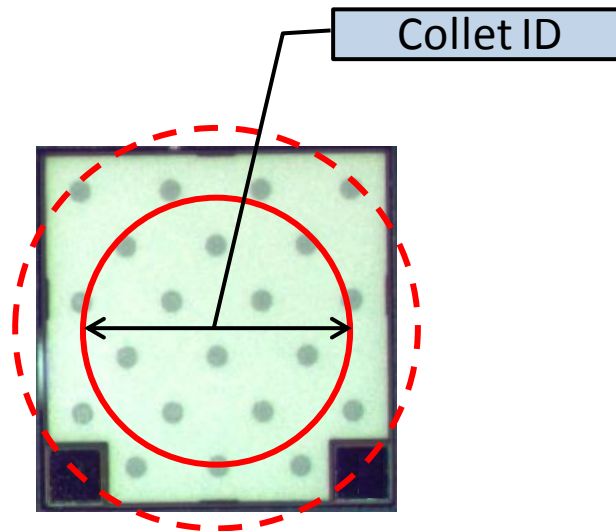
- Minimize ejector pin speed and travel
- Synchronize pin travel with collet motion to minimize the force applied to the chip
- If possible, adjust the ejection process to prevent pin penetration of the tape film



*Collets*

Rubber collets and handling fixtures with hardness in the approximate range of 80 (Shore A), or equivalent, are recommended. Harder plastic collets may also be used, in which case minimization of die placement or bonding parameters (forces) is recommended. The selection of bonding force level should be confirmed through reliability testing. A variety of rubber and plastic collet materials, covering a range of use temperatures, are available for use with EZ-p LEDs, including Teflon®, Vespel®, silicone rubber, and Viton®.

Recommended collet inner diameters (ID) for use with the corresponding EZ-p chip designs are listed in Table 2. Customers should contact the collet manufacturers for recommendations on designs specific to their application and die bonding equipment. Supplier information is provided following Table 2. For more information or questions regarding collet recommendations please contact Cree [www.cree.com](http://www.cree.com).



EZ-p Chip	Collet ID (µm)
Chip dimension < 400 µm	200-210
400 µm ≤ Chip dimension < 700 µm	400-420
700 µm ≤ Chip dimension ≤ 1400 µm	750-770
Chip dimension > 1400 µm	1500-1520

**Table 2: Collet ID recommendations**

Supplier Information

**Micro Mechanics** ([www.micro-mechanics.com](http://www.micro-mechanics.com)): Singapore, China, Taiwan, Japan

**Small Precision Tools (SPT)** ([www.smallprecisiontools.com](http://www.smallprecisiontools.com)): USA, Singapore, China, Japan

## EZ-p LED CHIP DIE ATTACH

### Eutectic/Solder Attach

For all solder attach processes the following guidelines must be observed:

- The maximum reflow process conditions for EZ-p LEDs are **325°C for 5 seconds**. This process window is adequate for the reflow of the intrinsic die attach metallization and a range of other solders, including Pb-free solders. It is recommended that temperature profiles be verified by **direct measurement** at the LED chip to ensure that the maximum process limits are not exceeded.
- If plasma cleaning is a customer consideration, Cree recommends that the devices not be exposed to Hydrogen plasmas. Addition of Hydrogen to other types of plasma should be minimized.
- Minimal pressure should be applied to the EZ-p chip during the soldering process. Pressure eutectic attach of EZ-p LEDs is not a Cree recommended process, however if the customer elects to use this process, then a maximum bonding force of **50 grams** is recommended.
- Complete solder underfill of the EZ-p chip is required, especially at the edges of chips with corner bond pads, to provide a rigid support to the chip for subsequent wirebonding.

### Flux

Recommended fluxes for EZ-p **flux eutectic attach (FEA)** are listed in Table 3 along with the manufacturer recommended cleaning agents. Alternative fluxes should be evaluated by the customer, as appropriate. Flux residue should be cleaned prior to encapsulation. Follow the flux manufacturer's recommended cleaning process or contact Cree for additional information ([www.cree.com](http://www.cree.com)).

Flux should be dispensed onto the substrate such that the EZ-p LED chip's anode metallization will have complete coverage. Avoid using excessive flux to prevent die movement during reflow. Flux quantity may be optimized by seating the EZ-p LED chip into the dispensed flux during die placement and minimizing the amount of flux displaced around the base of the die. The required quantity of dispensed flux may vary depending on the type of flux used and EZ-p chip size.

Flux	Cleaning Solution
Alpha Metal UP78-PT1	BIOACT® EC7-R™ or 10% Alpha® 2110 saponifier with water.
Indium Tac007	Kyzen® Ionox® I3302
Arakawa WHP-002/WHP-002 LED	PINE Alpha series

**Table 3: Recommended fluxes and cleaning agents**

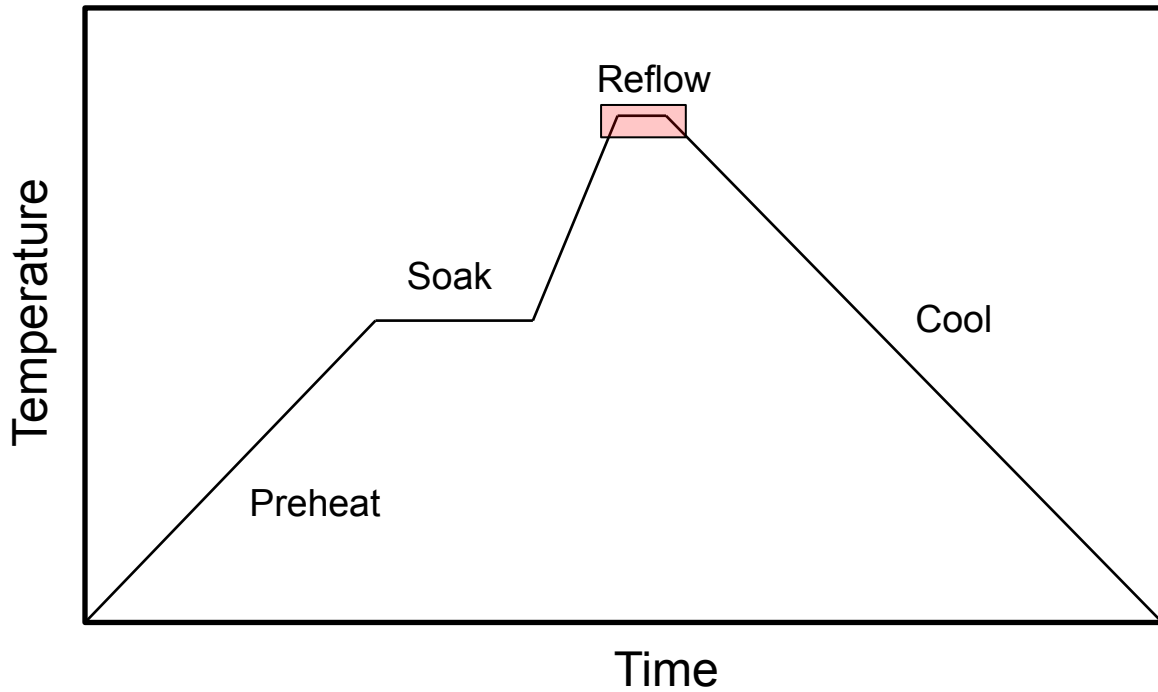
When using the intrinsic die attach metal for FEA Cree recommends the following guidelines for substrate metal finish to enable good surface wetting and uniform metal bond formation.

Design Item	Dimension (µm)
Substrate Roughness	Ra ~0.7, Rz < 2

**Table 4: Substrate surface finish parameters**

*Reflow*

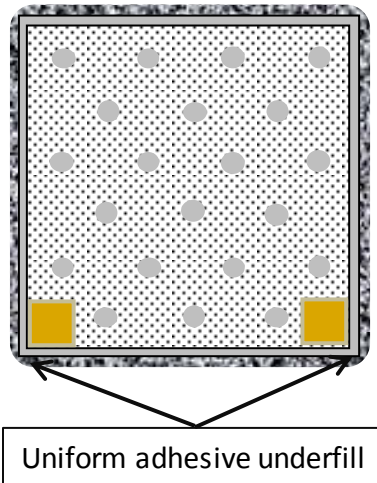
The reflow profile for EZ-p LED chips can vary depending on the thermal mass of the leadframe or substrate. A schematic reflow profile is shown below. Cree recommends that the pre-heat, thermal soak and cooling profile conform to the flux manufacturer’s recommendations. The target reflow zone for the intrinsic AuSn die-attach metallization should be limited to 300-320°C for less than 30 seconds.



*Adhesive Attach*

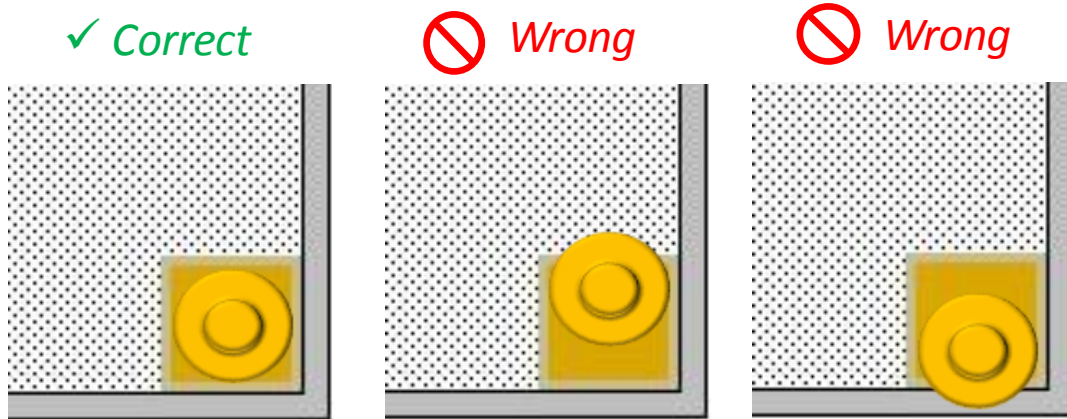
An electrically conductive adhesive must be used for EZ-p LED chips. It is important that the adhesive completely underfill the EZ-p LED chip, as this will ensure adequate die adhesion and will provide a rigid support to the chip during subsequent wirebonding. Adhesive should be visible around the entire periphery of the chip after die placement, especially at the edges of chips with corner bond pads, as shown below.

Conductive adhesive should not contact the top surface of the chip as this can lead to electrical leakage and reduced device performance.



**EZ-p LED WIRE BONDING**

EZ-p LED chips are designed for Au-ball wirebonding. Aluminum wedge bonding is not a Cree recommended process. It is important that the entire ball bond remain within the confines of the bond pad area and that no metal contact the emitting surface. Care must also be taken to prevent the wire capillary fixture from contacting the emitting surface as this can damage the LED junction. Several EZ-p LED chip designs feature bond pads adjacent to the edge of the junction mesa, therefore wirebonds must not exceed the bond pad area and lap over the edge of the mesa as this could lead to shunting leakage and/or junction damage.



The following guidelines should be observed for optimal wirebonding of EZ-p LED chips:

- Wirebonding force and ultrasonic power should be minimized
- Capillary geometry should be chosen to minimize the force required for ball formation
- Wirebonding process temperatures should be adjusted to minimize the required bonding forces/powers

Absolute bonding parameters for EZ-p LED chips cannot be specified since bonding equipment and materials vary greatly. Table 5 lists suggested maximum parameters that may be used as a guideline for wirebond development. The customer is advised to optimize bonding parameters for their specific equipment, tooling, and bonding wire.

Wirebonding Parameter *	Maximum Value
<b>Bond Time</b>	12 ms
<b>Bond Force</b>	40 g-force
<b>Ultrasonic Power</b>	100 mW
* Parameters based on settings for ASM Eagle 60 Au-ball bonder using AW99 1.2 mil Au wire at 160°C bonding temperature, Gaiser 1572-17-437GM-20D capillary, 138kHz ultrasonic frequency.	

**Table 5: Target wirebonding parameters**